

**What is claimed is:**

- 1     1.     A method for analyzing a semiconductor die having silicon-on-insulator (SOI)  
2     structure and a back side opposite circuitry near a circuit side, the method comprising:  
3             removing substrate from the back side of the semiconductor die and exposing a  
4     region of the insulator of the SOI structure where the substrate has been removed; and  
5             inducing a detectable response from the exposed region as a function of a  
6     portion of the circuitry and, therefrom, analyzing the die.
- 1     2.     The method of claim 1, wherein inducing a detectable response includes using  
2     an electron beam.
- 1     3.     The method of claim 2, further including detecting secondary electrons  
2     generated in response to the electron beam and the portion of the circuitry and wherein  
3     analyzing the die includes using a scanning electron microscope (SEM).
- 1     4.     The method of claim 3, wherein analyzing the die includes detecting a first  
2     magnitude of secondary electrons from a selected circuit portion and a second  
3     magnitude of secondary electrons detected from another circuit portion, the first and  
4     second magnitudes of secondary electrons being indicative of an electric characteristic  
5     differential between the selected circuit portion and the other circuit portion.

1 5. The method of claim 4, further comprising detecting secondary electrons from a  
2 plurality of circuit portions and obtaining an image of the die that represents variations  
3 in voltage across the plurality of circuit portions.

1 6. The method of claim 2, wherein using the electron beam includes pulsing the  
2 beam, and wherein analyzing the die includes obtaining a waveform response to the  
3 pulsed beam.

1 7. The method of claim 6, further comprising coupling a power supply to the die  
2 and inputting electrical signals to the die to generate a response.

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2 8. The method of claim 1, wherein inducing a detectable response includes  
3 inducing a response as a function of an electrical characteristic of a source/drain region  
4 in the die.

1 9. The method of claim 1, wherein inducing a detectable response includes using a  
2 buried oxide (BOX) portion of the SOI structure as a dielectric.

1 10. The method of claim 9, wherein removing a portion of substrate from the back  
2 side of the semiconductor die includes exposing a portion of the BOX.

1 11. The method of claim 1, wherein analyzing the die includes post-manufacturing  
2 analysis.

1 12. The method of claim 11, wherein analyzing the die includes obtaining a  
2 response for electrical stimulus applied to circuitry in the die.

1 13. The method of claim 12, wherein inputting electrical signals includes inputting  
2 signals known to induce a failure in the die.

1 14. The method of claim 12, wherein inputting electrical signals includes inputting  
2 signals in a continuous loop.

1 15. The method of claim 1, further comprising inducing a detectable response from  
2 a non-defective die in the same manner as the die being analyzed, the non-defective die  
3 having the same design as the die being analyzed, and comparing the analysis of the  
4 dies.

1 16. A system for analyzing a semiconductor die having silicon-on-insulator (SOI)  
2 structure and a back side opposite circuitry near a circuit side, the system comprising:  
3 means for removing substrate from the back side of the semiconductor die and  
4 exposing a region of the insulator of the SOI structure where the substrate has been  
5 removed;

6 means for inducing a detectable response from the exposed region as a function  
7 of a portion of the circuitry; and

8 means for detecting the response and, therefrom, analyzing the die.

1 17. A system for analyzing a semiconductor die having silicon-on-insulator (SOI)  
2 structure and a back side opposite circuitry near a circuit side, the system comprising:

3 a substrate removal arrangement adapted to remove substrate from the back side  
4 of the semiconductor die and expose a region of the insulator of the SOI structure where  
5 the portion has been removed;

6 a probe arrangement adapted to induce a detectable response from the exposed  
7 region as a function of a portion of the circuitry; and

8 a detector adapted to detect the response and, therefrom, analyze the die.

1 18. The system of claim 17, further comprising a controller adapted to control the  
2 substrate removal arrangement.

1 19. The system of claim 18, wherein the controller is adapted to control the substrate  
2 removal arrangement to remove sufficient substrate to facilitate the inducing of a  
3 response from the exposed region as a function of a portion of the circuitry.

1 20. The system of claim 17, wherein the substrate removal arrangement is adapted  
2 to remove enough substrate to expose a BOX portion of the SOI structure.

1 21. The system of claim 17, wherein the probe arrangement includes an SEM  
2 adapted to provide at least one of: an image of a circuit under analysis and data for  
3 probe navigation.

1 22. The system of claim 21, wherein the SEM also includes the detector and is  
2 further adapted to obtain an image of the die having light and dark areas, the dark areas  
3 being indicative of circuit portions having a positive voltage greater than that of lighter  
4 areas.

1 23. The system of claim 17, further comprising a tester adapted to introduce  
2 electrical stimulus to the die.

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